Amendments to the Specification:

In the RELATED PATENT APPLICATION, please replace the complete paragraph as follows:

This application is related to US patent application ~~docket number DS03-005A, US~~ Serial No. 10/764,914 _ filed concurrently herewith on Jan. 26, 2004 and ~~docket number DS03-006, US~~ patent application Serial No. 10/676919 _ filed on Oct. 1, 2003 and assigned to the same assignee as the present invention.

In the SUMMARY OF THE INVENTION,

after the first 2 paragraphs of this section, please add 2 new paragraphs as follows:

Within said set of small capacitors, one capacitor after the other is switched in parallel to change the total sum of capacitance. To achieve a linear capacitance change, said capacitors are not switched on one by one in digital steps, however each capacitor is switched on partially in a sliding operation, starting at low value (0 % of its capacitance) and ending with the fully switched on capacitor (100 % of its capacitance). To achieve said sliding switch operation, a typical implementation uses FET-transistors as switching device, one per capacitor. The switching operation of such FET-type transistor can be divided into three phases: the fully-switched-off phase (said FET transistor's drain-source-resistance RDS is very high), a steady ramp-up/ramp-down phase or steady transition phase (that is: said FET transistor's resistance RDS is changing between very high resistance and very low resistance in a linear and steady mode) and the fully-switched-on phase (said FET transistor's drain-source-resistance RDS is very low). By thoroughly controlling such switching device within said linear and

steady ramp-up/ramp-down phase, the capacitor in series with said switching device is partially switched in parallel with a well-controlled proportion between 0 % and 100 %.

The terms "steady ramp-up/ramp-down phase" or "steady transition phase" (and "steady ramp-up/ramp-down area" or "steady transition area") are used as synonyms throughout this document. The term "area" in this context is used to express the "operating range" – the term "phase" is used to express the "operation in process" within said operating area.

Please replace the paragraph, which was originally the 3rd paragraph of this section (and the first full paragraph on page 5) with the following amended paragraph:

One key point to obtain a high Q-factor is to drive the capacitor-switching element, typically a FET-transistor, into minimum RDSon or maximum RDSoff, as the parasitic resistance of RDS is the reason for Q-factor degradation. Another key point to obtain highest possible Q-factor: only very few transistors (ideally only one) should be in the ~~active operating mode~~ steady transition phase, i.e. in RDS~~on~~-changeing-mode, all others are either fully switched on or fully switched off. To achieve this goal, an individual threshold level for each capacitor switching stage defines the point where, in relation to the tuning voltage, each of said capacitor switching stages switches from the off to the on state. Overlapping of neighboring switching stages cannot be completely eliminated, but overlapping is kept to a minimum by selecting appropriate threshold parameters.

Please replace the last paragraph on page 5 with the following amended paragraph:

Furthermore, in a third solution according to the objectives of this invention, introduces a set of operational amplifiers, one for each capacitor-switching device. A resistor chain, or a similar circuit, produces a series of threshold points and each of said operational amplifiers compares the tuning voltage input with its dedicated ~~reference~~ threshold voltage. While said switching transistor is kept within its active switching range (RDS changing mode) the resistance of the transistor linearly follows the input difference of said operational amplifier. Said operational amplifiers give all freedom in circuit dimensioning to decide on the preferred threshold values and steepness of the switching ramp.

Please remove the 2nd full paragraph on page 6:

~~Depending on the technique to implement the reference values for each of the amplifiers within said operational amplifier chain, even specific nonlinear relations of capacitance change versus tuning voltage can be constructed.~~

Please replace the 3rd full paragraph on page 6 with the following amended paragraph:

In accordance with the objectives of this invention, a set of individual capacitors is implemented. Such capacitors could, ~~for example,~~ be discrete metal or polymer capacitors on a common planar carrier or they could be integrated on a semiconductor substrate. The switching device is typically a FET transistor, which could be for example a P-~~MOS~~channel or N-~~MOS~~channel junction FET or a P-~~channel~~MOS or N-~~channel C~~MOS FET.

Please replace the last paragraph starting on page 6 with the following amended paragraph:

In accordance with the objectives of this invention, a method to control the capacitance of a variable capacitor in a linear mode through a tuning voltage and to achieve a high Q-factor at the same time generate, is achieved. One method is to switch a variable number of capacitors in parallel, where only very few (ideally only one) are in the active transition phase of being switched on in a continuous mode. All other capacitors of a larger number of capacitors are either already fully switched on or are still complete switched off. One key method is to control the switching function for each of said ~~continual~~ switching devices, when said switching device is in its dedicated active working area in a linear mode. A further method amplifies, by the means of an operational amplifier, the difference of the capacitance tuning voltage and said ~~reference~~ threshold voltage of each amplifier stage, producing the linear control signal for said ~~continually~~ steady progressing switching operation. Another method generates a set of reference values, one for each of said amplifier stages. A tuning voltage is supplied to the circuit, dedicated for the voltage controlled capacitance change, to all of said amplifier stages.

In the BRIEF DESCRIPTION OF THE DRAWINGS.,
please replace the description of Fig. 9a with the following amended description:

Fig. 9a shows a circuit with operational amplifiers in the control signal path and with an alternative ~~reference voltage~~ threshold circuit.

please replace the description of Fig. 9b with the following amended description:

Fig. 9b shows the same circuit as Fig. 9a, additionally marking the areas of the Threshold Circuit, the Set of Switching Stages and the Set of Capacitors.

please replace the description of Fig. 10a with the following amended description:

Fig. 10a visualizes the overlapping switching operations of the individual stages of Fig. 9a.

please replace the description of Fig. 10b with the following amended description:

Fig. 10b shows the RDSon resistance versus the transistor's gate voltage for a single capacitor switching stage of Fig. 9a.

please replace the description of Fig. 11 with the following amended description:

Fig. 11 shows, in more detail, the gate voltage versus tuning voltage relation for the series of capacitor switching stages, according to Fig. 9a.

please replace the description of Fig. 12a with the following amended description:

Fig. 12a shows the capacitance versus tuning voltage for the series of capacitor switching stages, according to Fig. 9a.

please replace the description of Fig. 12b with the following amended description:

Fig. 12b shows the Q-factor versus tuning voltage for the series of capacitor switching stages, according to Fig. 9a.

please replace the description of Fig. 14 with the following amended description:

Fig. 14 visualizes the overlapping switching operations of just 2 stages of the circuit according to Fig. 9a.

Fig. 15a shows a realistic circuit diagram of an implementation, in accordance with an embodiment of this invention.

Fig. 15b shows the same circuit as in Fig. 15a, marking the circuit section of the Set of Capacitors, which could be implemented on a separate circuit carrier.

In the DESCRIPTION OF THE PREFERRED EMBODIMENTS,
please add the following 3 paragraphs after the first paragraph of this section (on page 11):

The variable capacitor arrangement implements a set of small capacitors, a set of capacitor switching stages and a circuit to provide a tuning voltage. To achieve the goal of high Q-factor, the disclosed invention adds circuits and methods to linearize the capacitance change and to minimize the effect of parasitic resistance in the capacitor switching elements, which would degrade the Q-factor.

Within said set of small capacitors, one capacitor after the other is switched in parallel to change the total sum of capacitance. To achieve a linear capacitance change, said capacitors are not switched on one by one in digital steps, however each capacitor is switched on partially in a sliding operation, starting at low value (0 % of its capacitance) and ending with the fully switched on capacitor (100 % of its capacitance). To achieve said sliding switch operation, a typical implementation uses FET-transistors as switching device, one per capacitor. The switching operation of such FET-type transistor can be divided into three phases: the fully-switched-off phase (said FET transistor's drain-source-resistance RDS is very high), a steady ramp-up/ramp-down

phase or steady transition phase (that is: said FET transistor's resistance RDS is changing between very high resistance and very low resistance in a linear and steady mode) and the fully-switched-on phase (said FET transistor's drain-source-resistance RDS is very low). By thoroughly controlling such switching device within said linear and steady ramp-up/ramp-down phase, the capacitor in series with said switching device is partially switched in parallel with a well-controlled proportion between 0 % and 100 %.

The terms "steady ramp-up/ramp-down phase" or "steady transition phase" (and "steady ramp-up/ramp-down area" or "steady transition area") are used as synonyms throughout this document. The term "area" in this context is used to express the "operating range" – the term "phase" is used to express the "operation in process" within said operating area.

please replace 4 paragraphs, beginning with the 2nd paragraph at page 12 with the following 4 amended paragraph:

A~~In a~~second solution according to the objectives of this invention, improves the circuit by introducing a voltage follower circuit **Vf** into the circuit of the first solution, as shown in **Fig. 6a**. For a single stage RDSon is forced to a linear mode of operation following **Vramp** through the whole working range between the power supply lines. The resulting **RDSon** versus the control voltage **Vramp** is shown in **Fig. 6b**.

When a capacitor tuning voltage is applied to the circuit of **Fig. 3**, the gate voltage **V1** to **Vn** of each individual switching device changes with a fraction of said tuning voltage, as visualized with lines **Vg1** to **Vg5** of **Fig. 7**. The threshold points are marked **Th1** to **Th5** in **Fig. 7** and the distance between threshold points are marked **d1**

to **d5**. A linear characteristic of the capacitance change is achieved when the resistors in said resistor chain in the circuit of **Fig. 3** are dimensioned to get threshold points with equal distance, i.e. when all threshold distances, symbolized as **d1** to **dn** in **Fig. 7**, are identical. In a circuit of **Fig. 3**, implementing a switching device as of **Fig. 5a** or **Fig. 6a**, the envisioned threshold voltages of **2% ON** and of **98% ON** shown in **Fig. 7** are in reality provided by the inherent switching characteristic of the switching devices implemented.

In a circuit that produces the individual control voltages for said capacitor switching devices with a mechanism similar to the resistor chain of **Fig. 3**, the next capacitor switching device in one stage starts to ramp up before the capacitor switching device in the previous stage reaches its endpoint. The ramps of both stages will therefore overlap. Said overlap, that increases with rising tuning voltage, will cause more and more switching devices to operate in their active working range, and as a result the Q-factor decreases continuously. The Q-factor degrading is shown in **Fig. 8**. Said increasing overlapping applies to a circuit according to **Fig. 3**, using the simple switching device of **Fig. 5a**, and ~~also~~ very similar applies to a circuit with voltage followers in the signal path, as of **Fig. 6a**.

In a third solution, a major improvement is achieved, by introducing an operational amplifier into the signal path, one for each capacitor-switching ~~device~~ stage. Further, the arrangement of the ~~reference voltage~~ threshold circuit is considerably improved. A resistor chain, or a similar circuit, produces a series of voltage references, used as threshold values, and each of said operational amplifiers compares the tuning voltage input with its dedicated ~~reference voltage~~threshold value. **Fig. 9a** shows a

principal diagram of such circuit. **Amp 1** to **Amp n** are said operational amplifiers, **Sw 1** to **Sw n** are the switching devices and **Cap 1** to **Cap n** are said capacitors that will be switched in parallel. **R1** to **Rn** build the resistor chain to produce references voltages **Ref 1** to **Ref n**. The resulting variable capacitance is available at the output points **varCap**. Fig. 9b identifies the major circuit sections within the circuit of **Fig. 9a**: the Threshold Circuit is marked **ThrC**, the Set of Switching Stages is marked **SoSWST** and the Set of Capacitors is marked **SoCAPS**.

please replace the 1st paragraph at page 14 with the following amended paragraph:

The ~~amplifiers~~switching slopes at adjacent capacitor switching stages need to slightly overlap to get a smooth linear capacitance curve, as shown in **Fig. 10a**. **Fig. 10b** visualizes the principal RDSon characteristic versus gate voltage of a single capacitor switching stage according to Fig. 9a. A more detailed view on the individual ramp-up functions at the switching transistor's gate is shown in **Fig. 11**. **Vg1** to **Vg7** are the gate voltage versus tuning voltage slope of the switching stages number 1 to 7 in this example. One can assume the active area of RDS changing to be between the 2 % point and the 98 % point. Compared to the characteristic of **Fig. 7**, all slopes of the individual gate voltages in **Fig. 11** are strictly parallel, which makes it easier to achieve the goal of linearity in the capacitor variation. Threshold points **Th1** to **Th7** in **Fig. 11** are equally spaced (distances **d1** to **d7** in **Fig. 11**).

please replace the last paragraph beginning at page 14 with the following amended paragraph:

Fig. 14 visualizes the overlapping switching operations of just 2 stages of the circuit according to Fig. 9a. **Overlap** is a measure, where **Vg2** just starts to switch on

stage number 2 and where **Vg1** is still in the active working range for stage number 1. Because said gate voltage versus tuning voltage slopes are all in parallel, all overlaps are the same.

please replace the 1st and 2nd full paragraph at page 15 with the following 2 amended paragraphs:

A major advantage of the circuit of **Fig. 9a**, which uses operational amplifiers to compare tuning voltage to an individual ~~reference~~ threshold voltage is, that all slopes of the gate control voltage and therefore the slopes of the RDSon variation are identical for all capacitance switching stages. Said slopes of the gate control voltage are shown in **Fig. 14**. In contrast to this, the slopes of the gate control voltage in a circuit, where a circuit produces the individual control voltages for said capacitor switching devices with a mechanism similar to the resistor chain of **Fig. 3**, all of said slopes are different. **Fig. 13** shows this typical behavior for the slopes of 3 neighboring stages

Fig. 15 shows a realistic circuit diagram of an implementation, in accordance with an embodiment of this invention. **Amp 1** to **Amp n** are said operational amplifiers, **Sw 1** to **Sw n** are the switching devices and **Cap 1** to **Cap n** are said capacitors that will be switched in parallel, resulting in the total capacitance **varCap**. **R1** to **Rn** build the resistor chain to produce references voltages for the translinear amplifiers of each stage, as already shown in **Fig. 9a**.

please remove the last paragraph at page 15:

~~Depending on the technique to implement the reference values for each of the amplifiers within said translinear amplifier chain, even specific nonlinear relations of capacitance change versus tuning voltage can be constructed.~~

please split the 1st full paragraph at page 16 into 2 paragraphs as indicated below and replace the resulting 2 paragraphs with the following amended 2 paragraphs:

In accordance with the objectives of this invention, a set of individual capacitors is implemented. **Fig. 15a** suggests, said set of capacitors could be integrated together with the capacitor switching stages on the same semiconductor substrate. However, s~~S~~uch capacitors **Cap 1** to **Cap n** could, for example, be discrete metal or polymer capacitors, on a common planar carrier or they could be integrated on ~~a~~ their own semiconductor substrate, which is separate from the semiconductor substrate of said capacitor switching stages. Manufacturing the capacitors in a different process than by integrating the capacitances together with the switch control circuit on the same semiconductor substrate, could lead to significant better quality of the capacitors. The circuit sections of said Set of Capacitors, that could be produced on a separate carrier, is marked **SoCAPS** on **Fig. 15b**; said separate carrier then connects to the remainder of the whole circuit through the connectors **Conn.**

The advantage of a capacitor not being of the junction (diode) type capacitor is the invariance due to voltage or temperature change at the capacitor. The switching device is typically a FET transistor, which could be for example a P-~~MOS~~channel or N-~~MOS~~channel junction FET or a ~~C~~PMOS or NMOS FET.